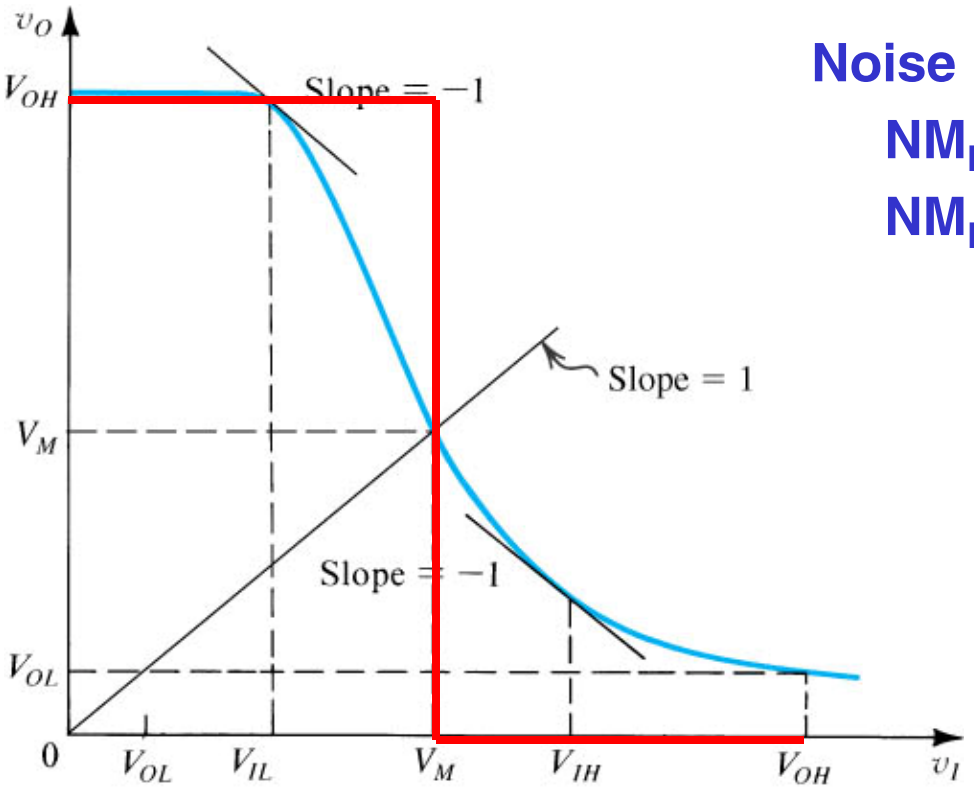
CHAPTER 10

# Digital CMOS Logic Circuits

## 10.1.1 Logic-Circuit Characterization: Noise Margin




**Noise Margin:**

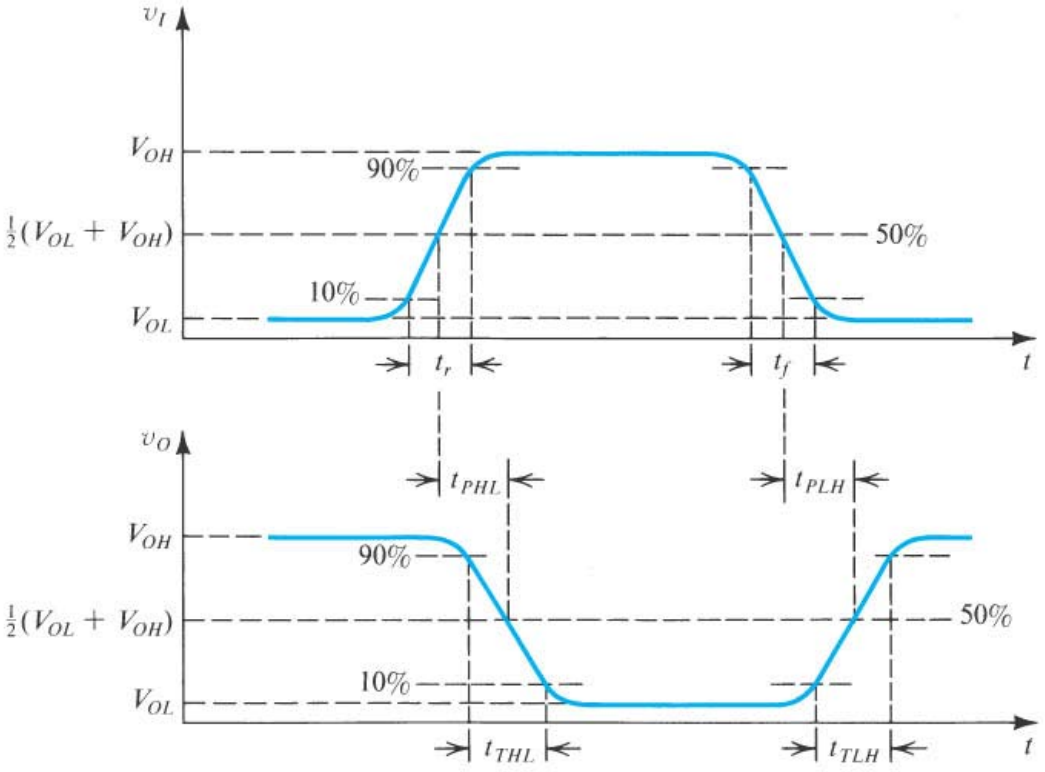
$$NM_H \equiv V_{OH} - V_{IH}$$

$$NM_L \equiv V_{IL} - V_{OL}$$

**Ideal Inverter:**

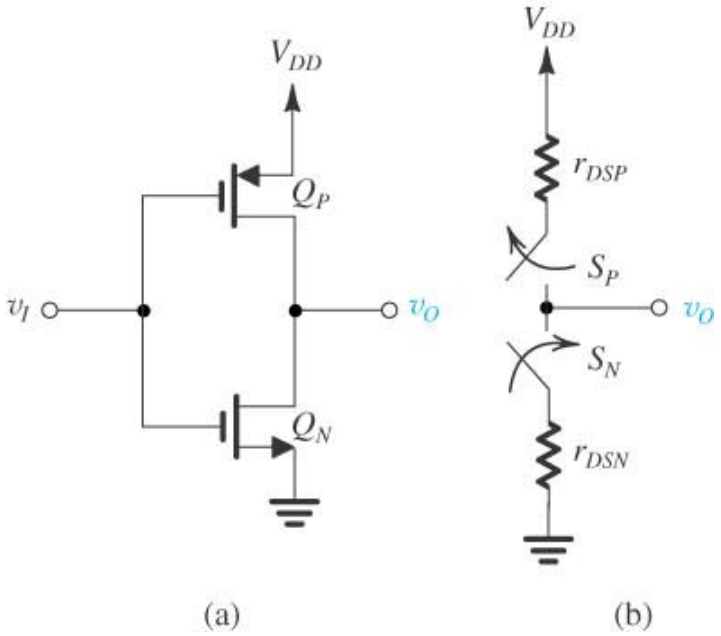
$$NM_H = NM_L = V_{DD}/2$$

## 10.1.1 Logic-Circuit Characterization: Propagation Delay




$$t_P \equiv \frac{1}{2}(t_{PLH} + t_{PHL})$$

## 10.2.1 Circuit Structure



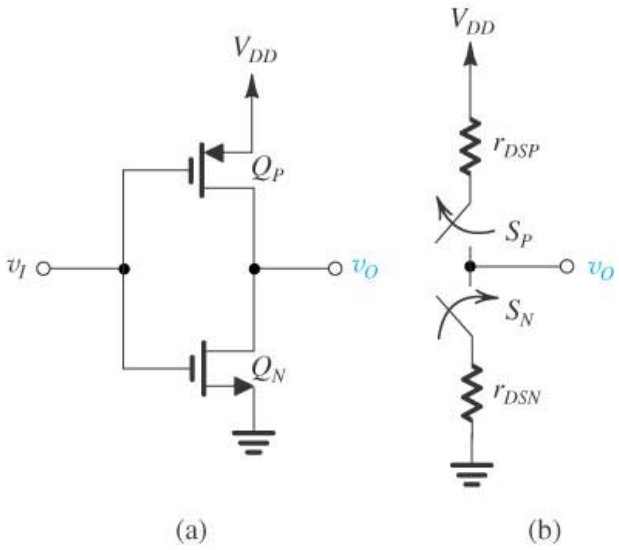

Triode: $i_D = k_n' \left(\frac{W}{L}\right)\left[(v_{GS} - V_T)v_{DS} - \frac{1}{2}v_{DS}^2\right]$

Saturation: $i_D = \frac{1}{2}k_n' \left(\frac{W}{L}\right)(v_{GS} - V_T)^2$

$$r_{DSN} \cong \frac{v_{DS}}{i_D} = \left[k_n' \left(\frac{W}{L}\right)_N (v_{DD} - V_t)\right]^{-1}$$

$$r_{DSP} = \left[k_n' \left(\frac{W}{L}\right)_P (v_{DD} - V_t)\right]^{-1}$$

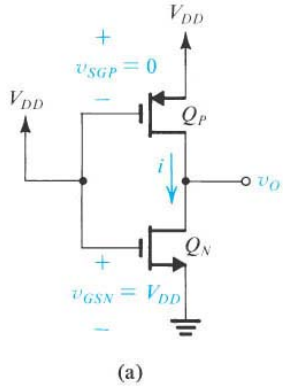
## 10.2.2 Static Operation



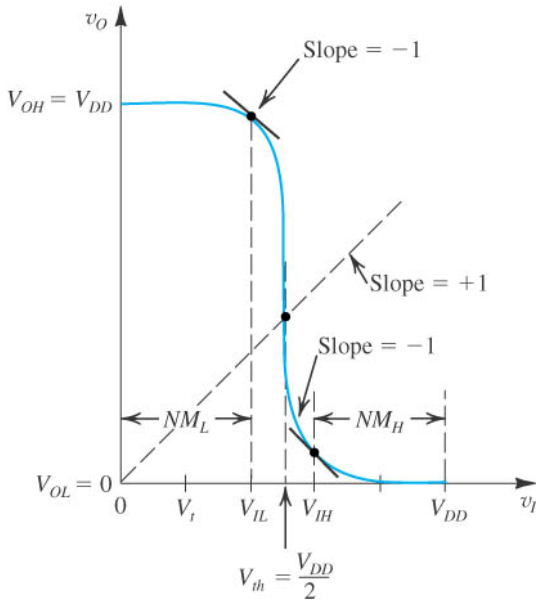

$$\begin{cases} v_I = 0, v_O = V_{DD} \\ v_I = V_{DD}, v_O = 0 \end{cases}$$

Static-power dissipation is zero

## 10.2.2 Static Operation: sizing the transistor




(a)




$$V_{th} = \frac{V_{DD} - |V_{tp}| + \sqrt{k_n / k_p} V_{tn}}{1 + \sqrt{k_n / k_p}}$$

$$k_n = k_n'(W/L)_n = C_{ox}\mu_n(W/L)_n$$

$$k_p = k_p'(W/L)_p = C_{ox}\mu_p(W/L)_p$$

For: $V_{tn} = |V_{tp}|, k_n = k_p$

$$V_{th} = V_{DD}/2$$

$r_{DSN}=r_{DSP}$:
**Equal propagation delay**

$$\mu_n(W/L)_n = \mu_p(W/L)_p$$

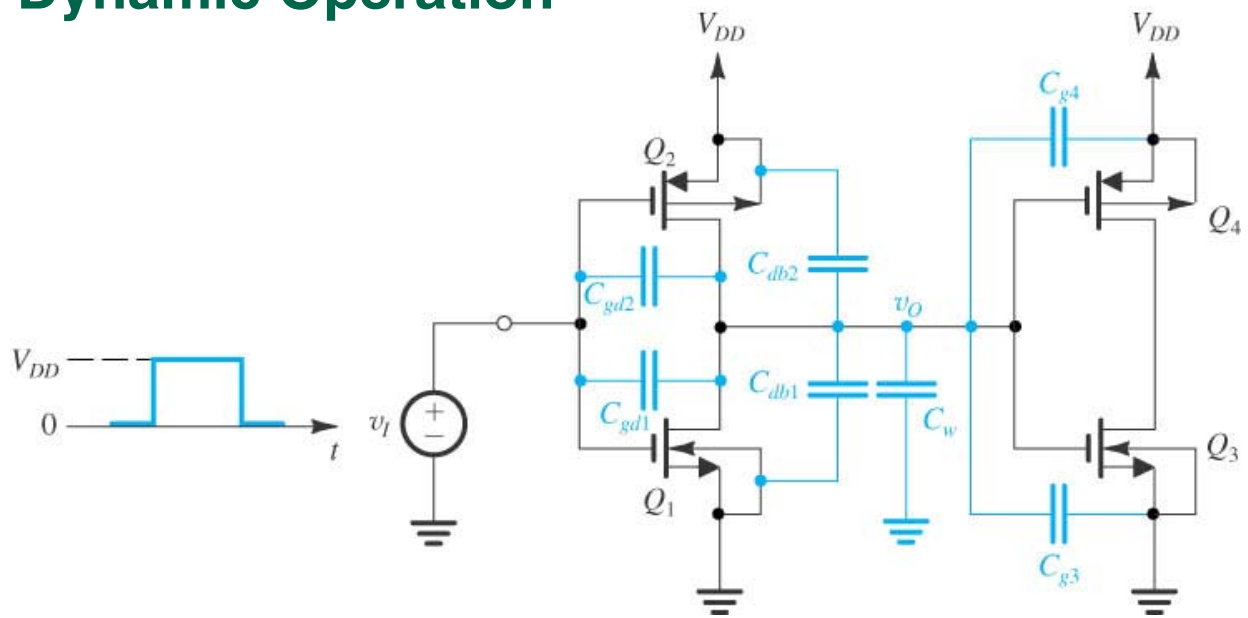
$$\left(\frac{W}{L}\right)_p = \frac{\mu_p}{\mu_n}\left(\frac{W}{L}\right)_n$$

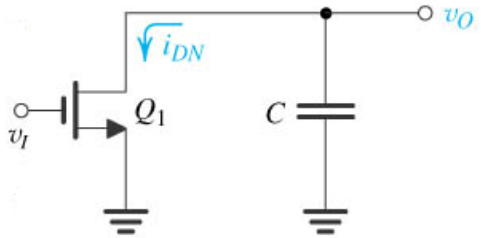
**Equal Noise Margin**

Area : $WL$

$$W_n L_n + W_p L_p = (W_n + W_p)L$$

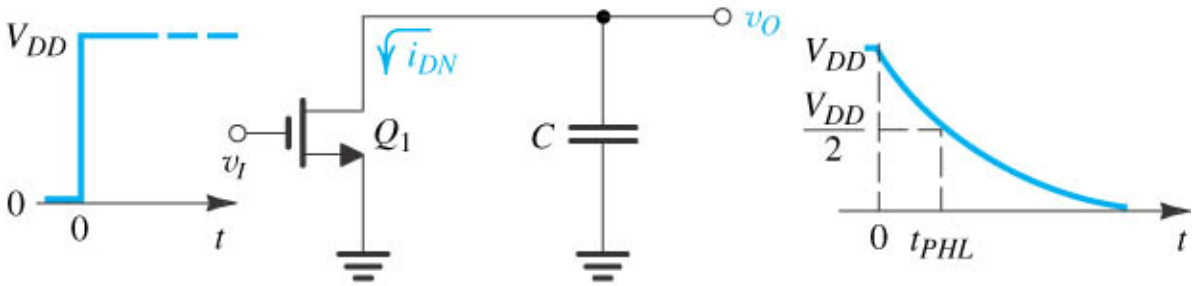
## 10.2.3 Dynamic Operation




$$C = 2C_{gd1} + 2C_{gd2} + C_{db1} + C_{db2} + C_{g3} + C_{g4} + C_w$$

## 10.2.3 Dynamic Operation




(a)

$$t = 0, \quad Q_1 : \text{Saturation} \rightarrow i_{D1}(0) = \frac{1}{2} K_n' \left(\frac{W}{L}\right)_n (V_{DD} - V_t)^2$$

$$t = t_{PHL}, Q_1 : \text{Triode} \rightarrow i_{D1}(t_{PHL}) = K_n' \left(\frac{W}{L}\right)_n \left[ (V_{DD} - V_t)\frac{V_{DD}}{2} - \frac{1}{2}\left(\frac{V_{DD}}{2}\right)^2 \right]$$

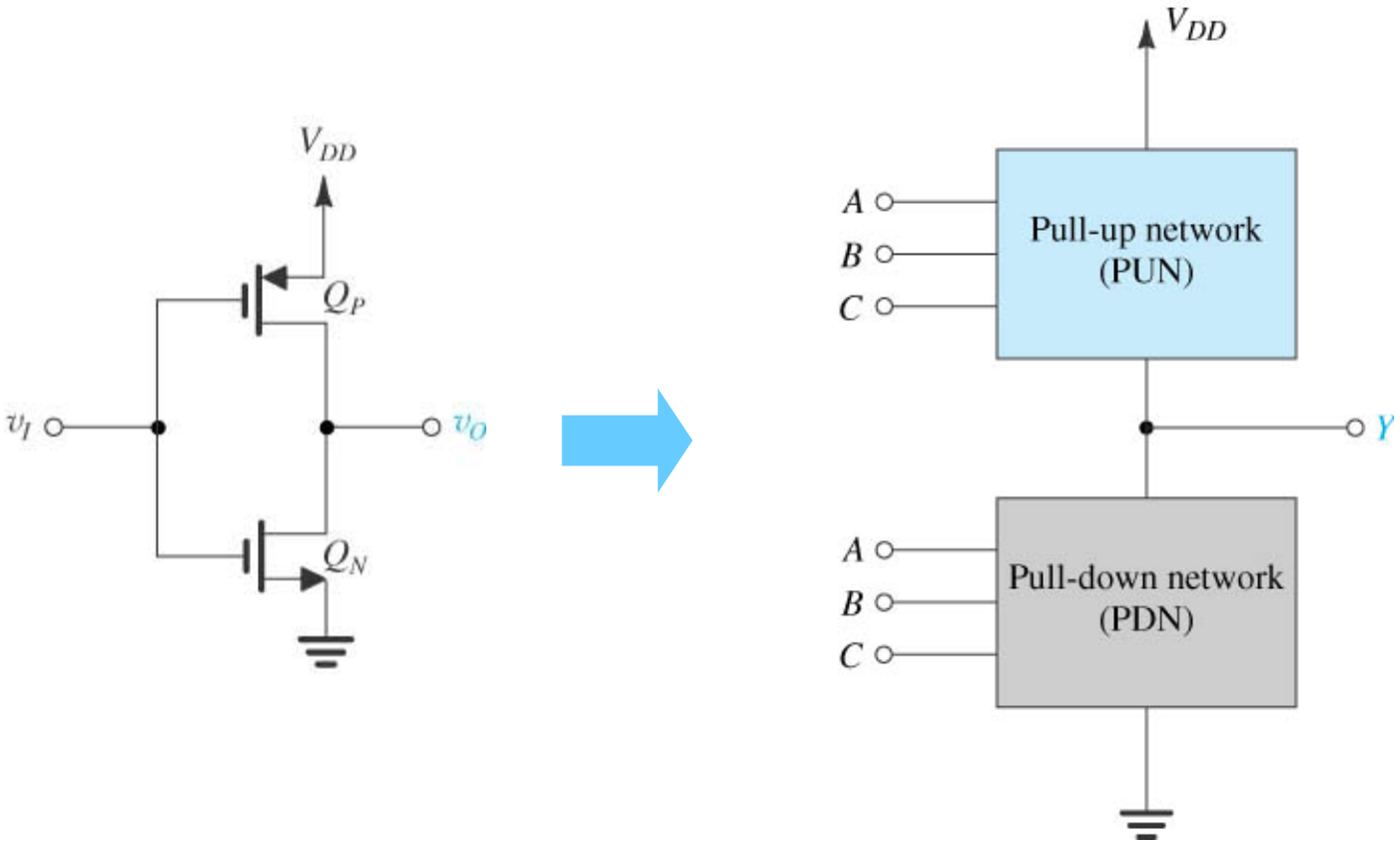
$$i_{D1}\big|_{av} = \frac{1}{2}\left[i_{D1}(0) + i_{D1}(t_{PHL})\right]$$

$$t_{PHL} = \frac{C\Delta V}{i_{D1}\big|_{av}} = \frac{CV_{DD}/2}{i_{D1}\big|_{av}} \overset{V_t = 0.2V_{DD}}{\cong} \frac{1.7C}{K_n'(W/L)_n V_{DD}}$$

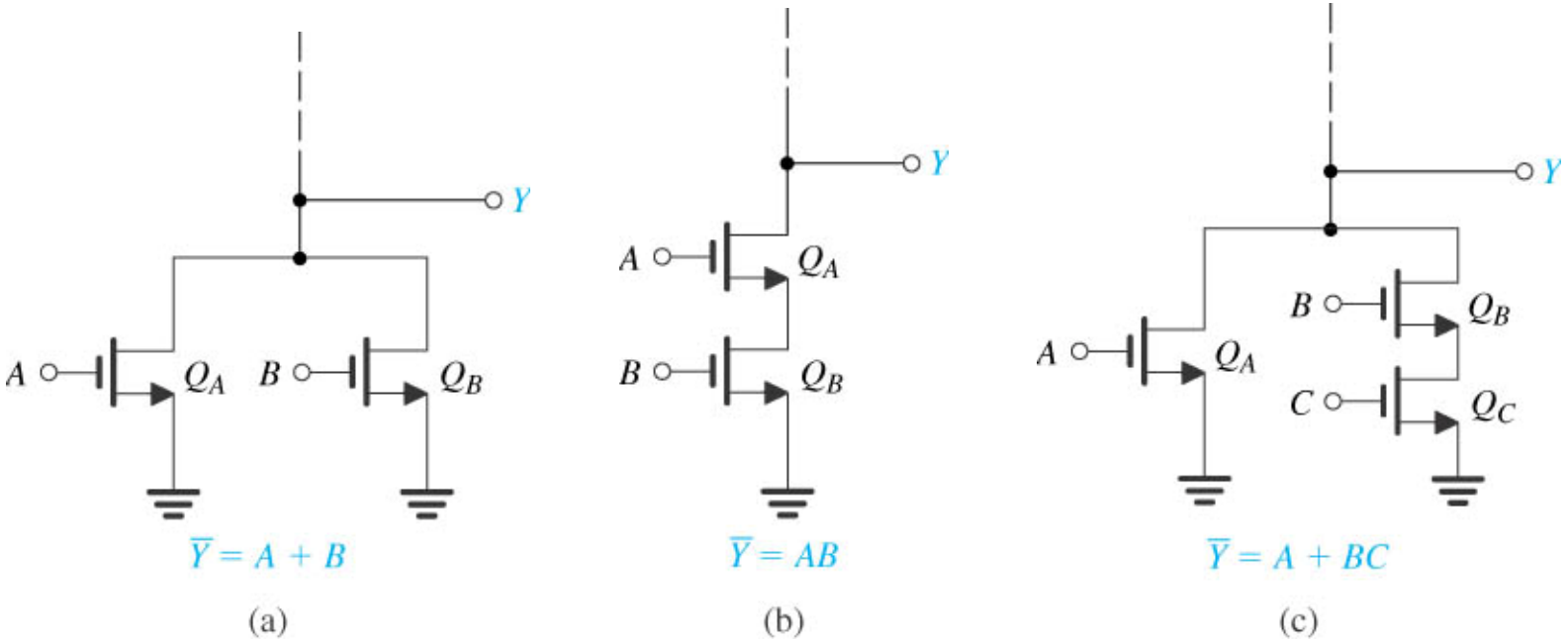
$$V_t \cong 0.2V_{DD}$$

$$t_{PHL} = \frac{1.6C}{K_n'(W/L)_n V_{DD}}$$

## 10.3.1 Basic Structure



## 10.3.1 Basic Structure (cont.)



# Homework:

**10.1, 10.6, 10.12, 10.16, 10.22, 10.25, 10.28**