

# CHAPTER 7

## Differential and Multistage Amplifiers

## 7.7 Multistage Amplifiers

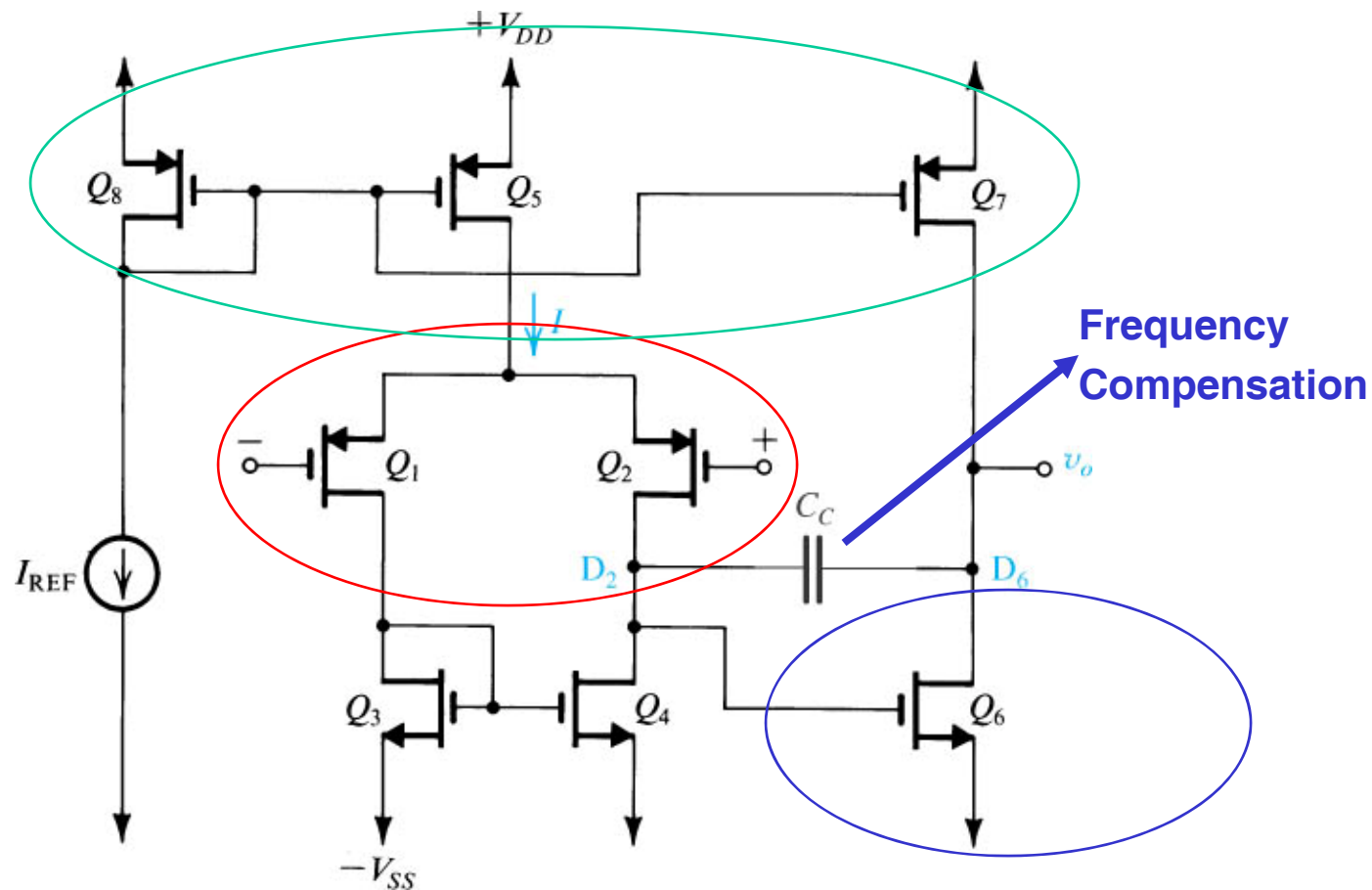
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### Why Multistage Amplifiers?

- The first stage is usually required to provide a *high input resistance* in order to avoid loss of signal level when the amplifier is fed from a high resistance source
- In a differential amplifier the input stage must also provide *large common-mode rejection*
- The middle stage is to provide the *bulk of the voltage gain*, conversion of the signal from differential mode to single-ended mode, and the shifting of the DC: allow output to swing both positive and negative
- Final stage is to provide a *low output resistance* in order to avoid loss of gain when load resistance is low: source follower / emitter follower

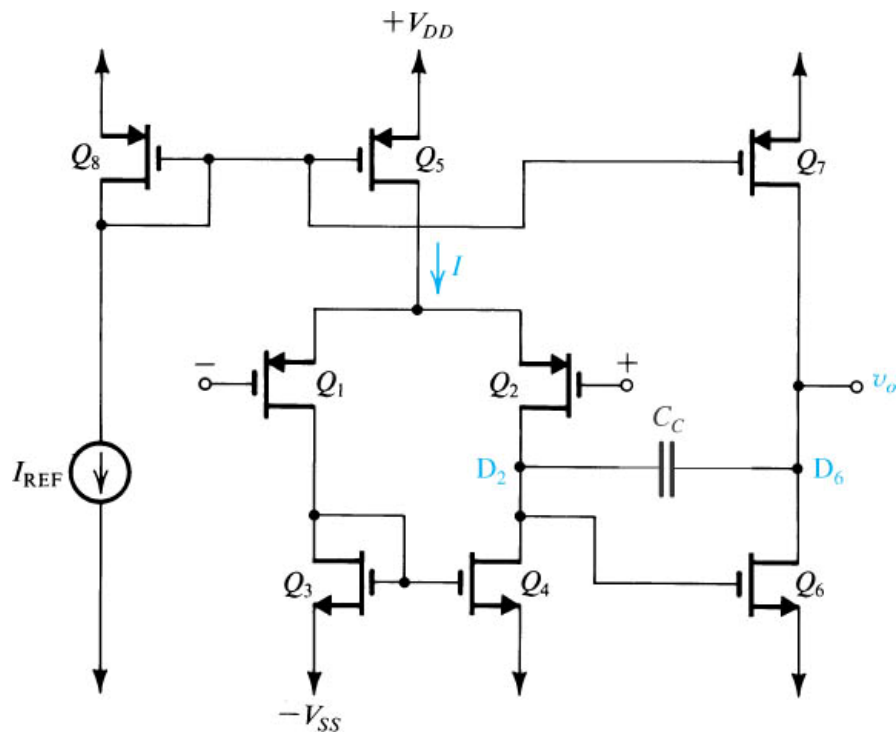
# 7.7 Multistage Amplifiers

## 7.7.1 A Two-Stage CMOS Op Amp



# 7.7 Multistage Amplifiers

## 7.7.1 A Two-Stage CMOS Op Amp – Voltage Gain



**First Stage:**

$$A_1 = -g_{m1}(r_{o2} \parallel r_{o4}) \quad (7.146)$$

**Second Stage:**

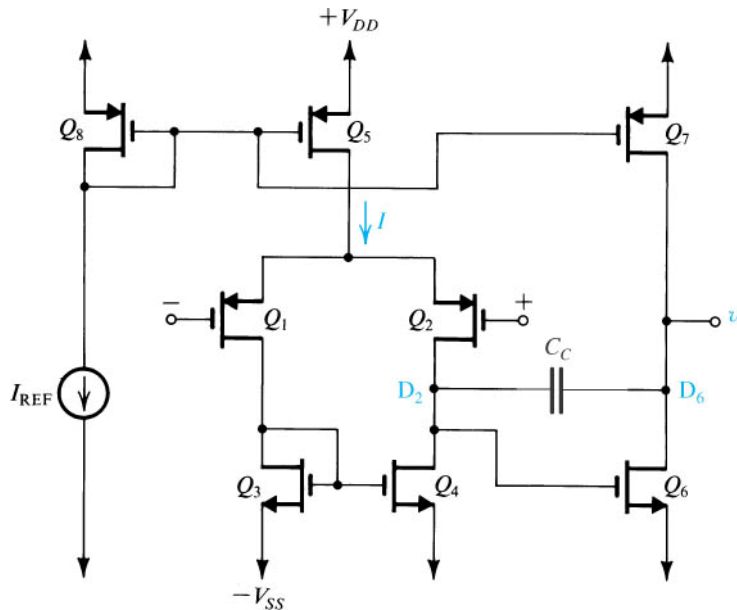
$$A_2 = -g_{m6}(r_{o6} \parallel r_{o7}) \quad (6.49)$$



# 7.7 Multistage Amplifiers

## Example 7.3

Find  $I_D$ ,  $|V_{OV}|$ ,  $|V_{GS}|$ ,  $g_m$ ,  $r_o$ ,  $A_1$ ,  $A_2$ .



	Q <sub>1</sub>	Q <sub>2</sub>	Q <sub>3</sub>	Q <sub>4</sub>	Q <sub>5</sub>	Q <sub>6</sub>	Q <sub>7</sub>	Q <sub>8</sub>
W/L	20/0.8	20/0.8	5/0.8	5/0.8	40/0.8	10/0.8	40/0.8	40/0.8
I <sub>D</sub> (μA)	45	45	45	45	90	90	90	90
V <sub>OV</sub>  (V)	0.3	0.3	0.3	0.3	0.3	0.3	0.3	0.3
V <sub>GS</sub>  (V)	1.1	1.1	1	1	1.1	1	1.1	1.1
g <sub>m</sub> (mA/V)	0.3	0.3	0.3	0.3	0.6	0.6	0.6	0.6
r <sub>o</sub> (Ω)	222k	222k	222k	222k	111k	111k	111k	111k

$$I_{REF} = 90 \mu\text{A}, V_{in} = 0.7\text{V}, V_{tp} = -0.8\text{V}$$

$$\mu_n C_{ox} = 160 \mu\text{A}/\text{V}^2, \mu_p C_{ox} = 40 \mu\text{A}/\text{V}^2$$

$$|V_A| = 10\text{V}, V_{DD} = V_{SS} = 2.5\text{V}$$

$$I_D = \frac{1}{2} (\mu C_{ox}) (W/L) V_{ov}^2 \quad |V_{GS}| = |V_{ov}| + |V_t| \quad g_m = 2I_D / |V_{ov}| \quad r_o = |V_A| / I_D$$

$$A_1 = -g_{m1} (r_{o2} \parallel r_{o4}) = -33.3\text{V}/\text{V}$$

$$A_2 = -g_{m6} (r_{o6} \parallel r_{o7}) = -33.3\text{V}/\text{V}$$

# 7.7 Multistage Amplifiers

## Example 7.3

The lower limit of the input common-mode is the value at which  $Q_1$  and  $Q_2$  leave the saturation region:

$$V_{D1} = -2.5 + 1 = -1.5V$$

$$V_{in\_lower} = -1.5 - 0.8 = -2.3V$$

The upper limit of the input common-mode is the value at which  $Q_5$  leaves the saturation region:

$$V_{SD5} = 0.3V \Rightarrow V_{D5} = 2.5 - 0.3 = 2.2V$$

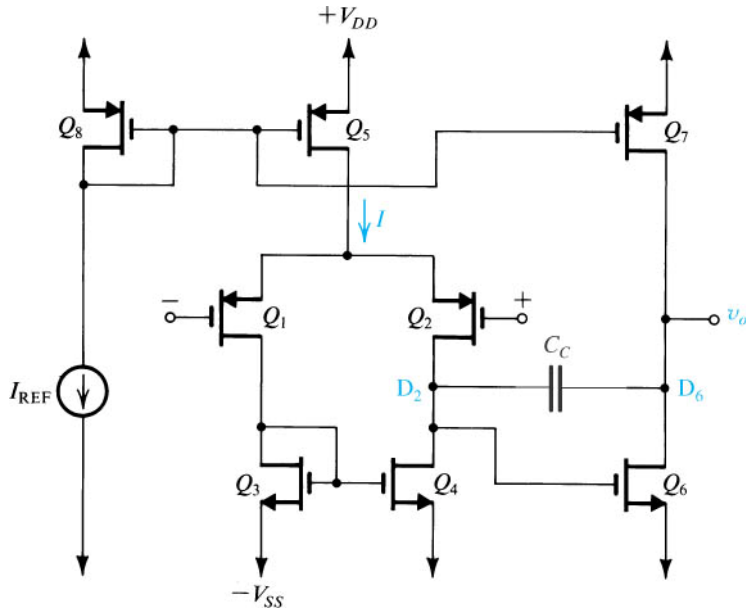
$$V_{S1} = V_{D5} = 2.2V$$

$$V_{GS1} = -1.1V \Rightarrow V_{G1} = 2.2 - 1.1 = 1.1V$$

$$V_{in\_upper} = 1.1V$$

**Highest output:**  $V_{DD} - |V_{OV7}| = 2.5 - 0.3 = 2.2V$

**Lowest output:**  $-V_{SS} + |V_{OV6}| = -2.5 + 0.3 = -2.2V$

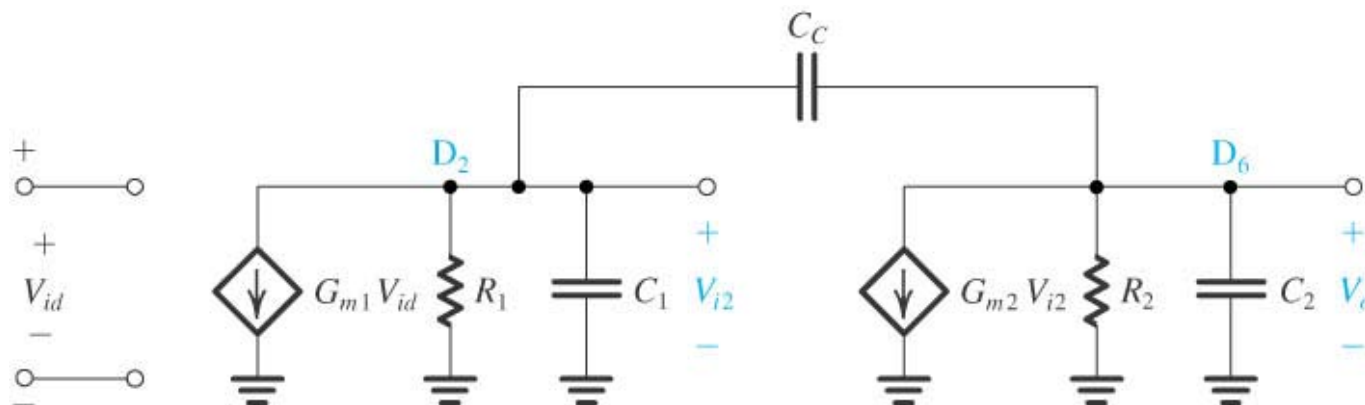


$$v_{GD} < V_t \Leftrightarrow v_{DS} < v_{GS} - V_t \Leftrightarrow v_{DS} < V_{OV}$$

PMOS:  $v_{SD} < |V_{OV}|$

## 7.7 Multistage Amplifiers

### 7.7.1 A Two-Stage CMOS Op Amp: Frequency Response

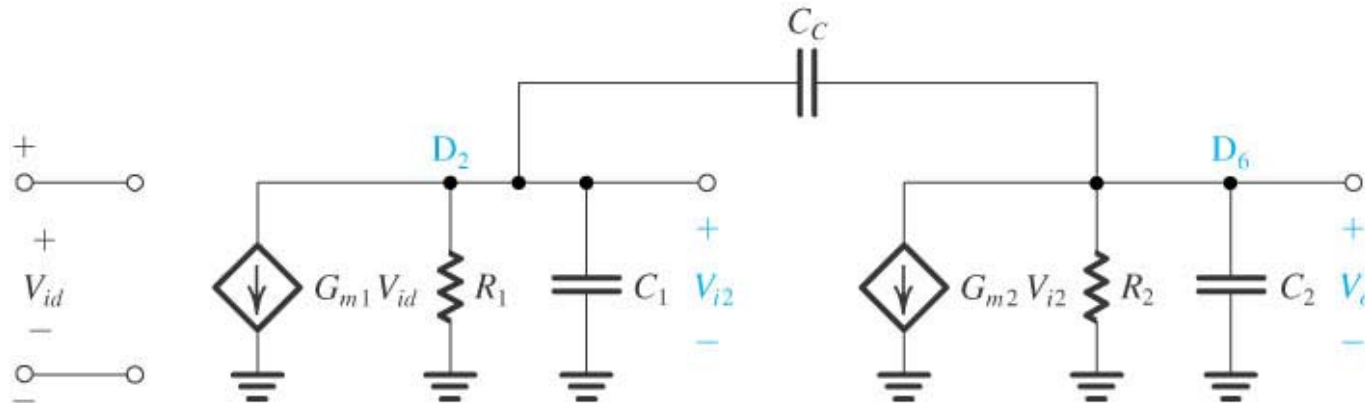


$$C_1 = C_{gd4} + C_{db4} + C_{gd2} + C_{db2} + C_{gs6}$$

$$C_2 = C_{db6} + C_{db7} + C_{gd7} + C_L$$

# 7.7 Multistage Amplifiers

## 7.7.1 A Two-Stage CMOS Op Amp: Frequency Response (cont.)



$$G_{m1}V_{id} + \frac{V_{i2}}{R_1} + sC_1V_{i2} + sC_C(V_{i2} - V_o) = 0$$

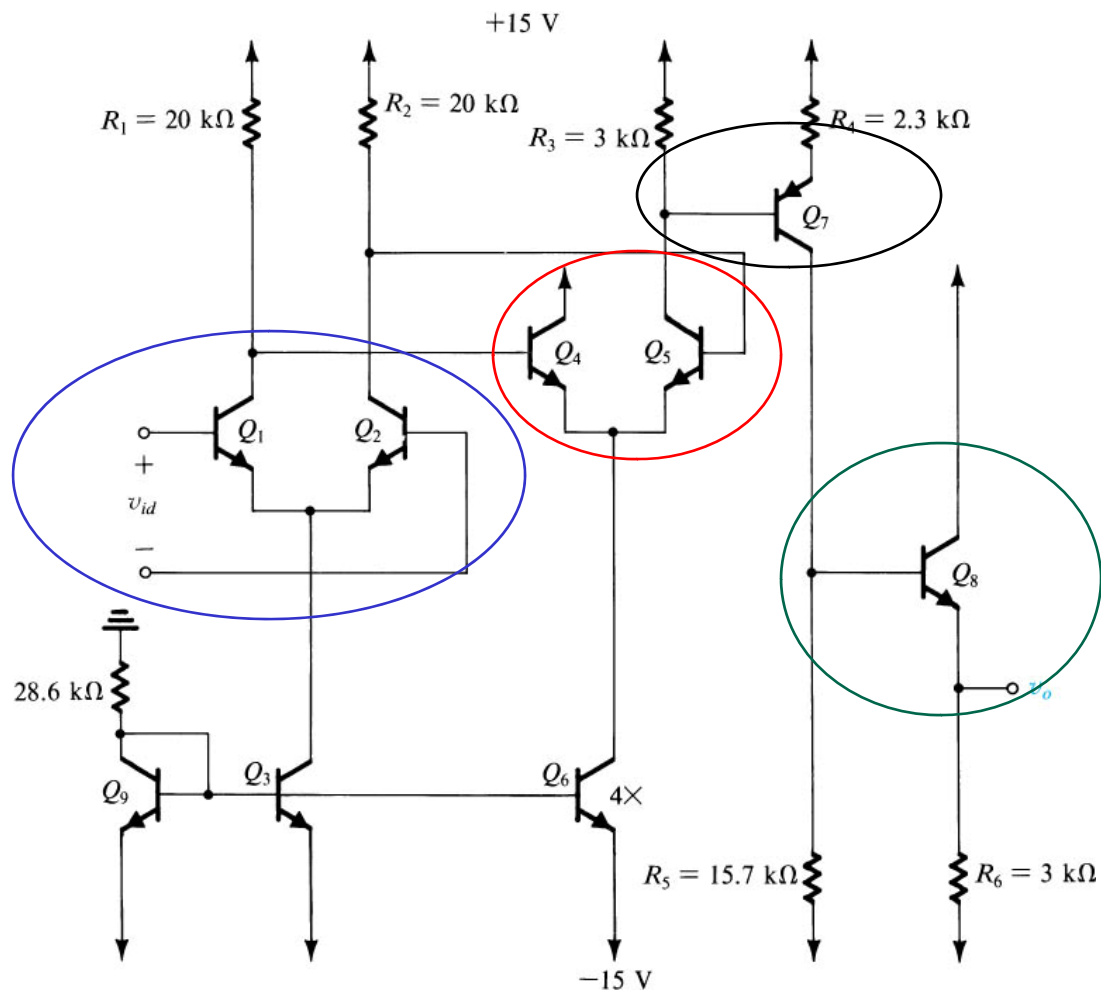
$$G_{m2}V_{i2} + \frac{V_o}{R_2} + sC_2V_o + sC_C(V_o - V_{i2}) = 0$$

$$\frac{V_o}{V_{id}} = \frac{G_{m1}(G_{m2} - sC_C)R_1R_2}{1 + s[C_1R_1 + C_2R_2 + C_C(G_{m2}R_1R_2 + R_1 + R_2)] + s^2[C_1C_2 + C_C(C_1 + C_2)]R_1R_2}$$

$\omega_{p1}$

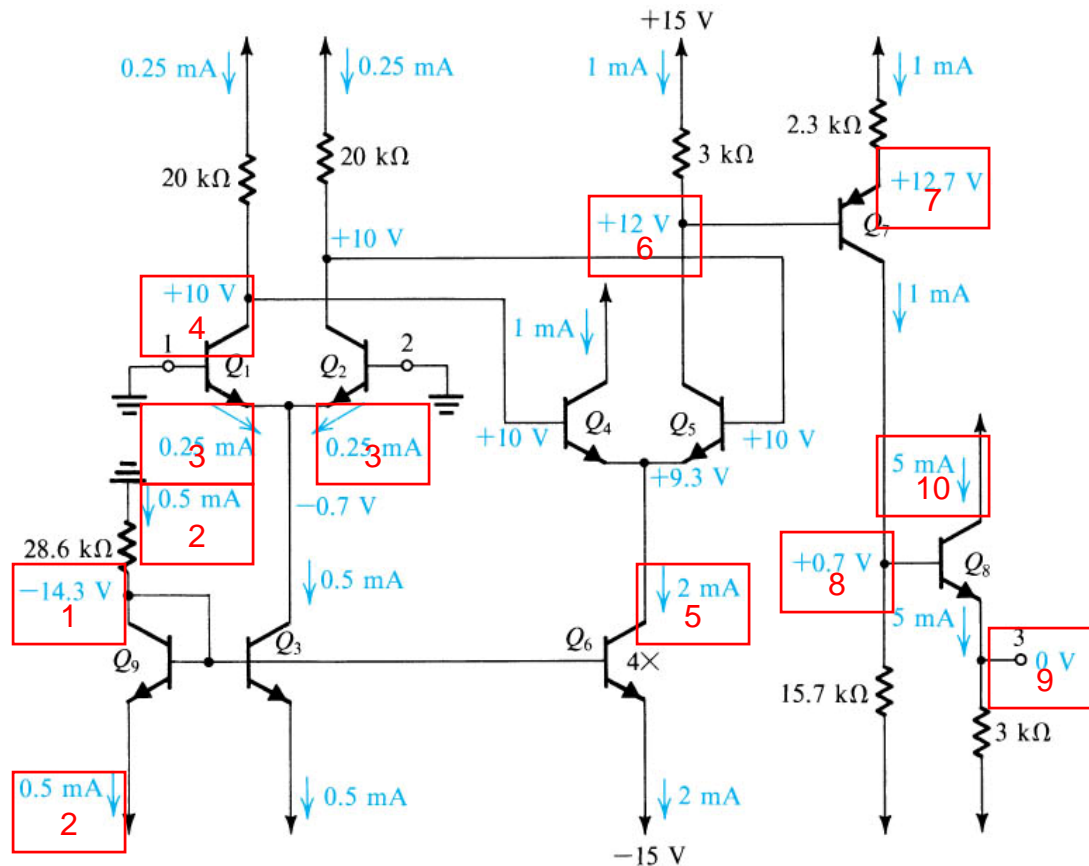
# 7.7 Multistage Amplifiers

## 7.7.2 A Bipolar Op Amp



# 7.7 Multistage Amplifiers

## 7.7.2 A Bipolar Op Amp (cont.)



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# Homework

**7.80, 7.85, 7.88, 7.92, 7.93, 7.94, 7.97**