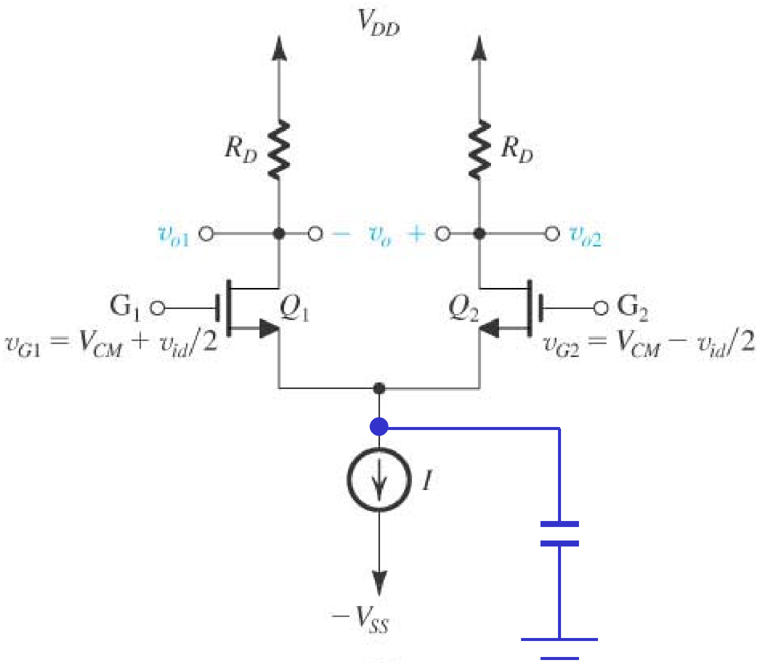
CHAPTER 7

Differential and Multistage Amplifiers

7.2.1 Differential Gain



(a)

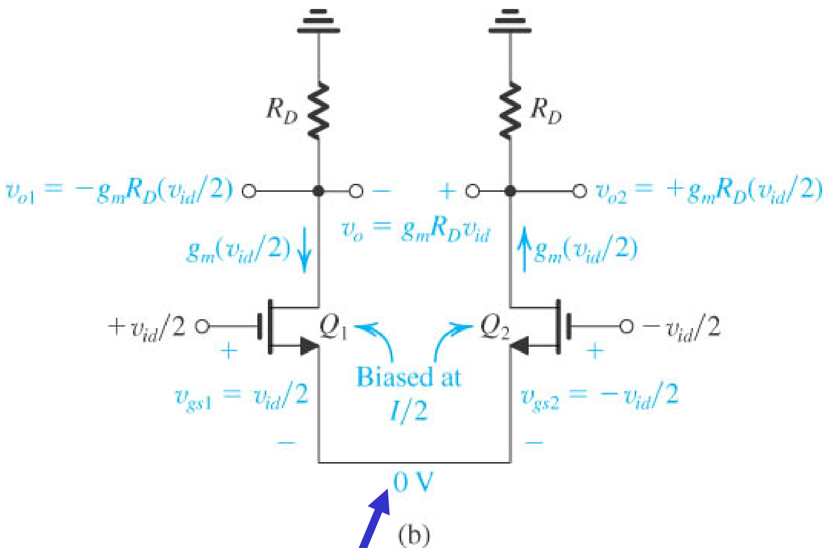
$$v_{G1} = V_{CM} + \frac{1}{2} v_{id}$$

$$v_{G2} = V_{CM} - \frac{1}{2} v_{id}$$

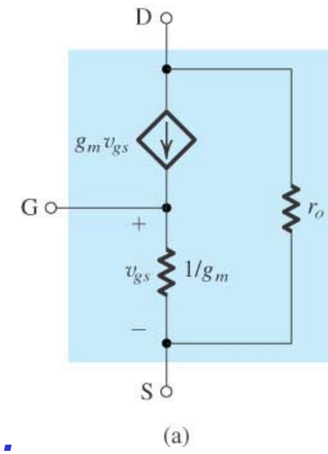
V_{CM} : Common - mode DC voltage

single-ended output v.s. differential output

7.2.1 Differential Gain (cont.)



Virtual Ground, NO capacitor!



Neglect r_o:

$$v_{o1} = -i_{d1}R_D = -\frac{v_{id}/2}{1/g_m}R_D = -g_m R_D v_{id}/2$$

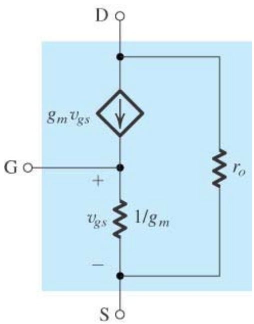
$$v_{o2} = -i_{d2}R_D = -\frac{-v_{id}/2}{1/g_m}R_D = g_m R_D v_{id}/2$$

$$\frac{v_{o1}}{v_{id}} = -\frac{1}{2}g_m R_D \qquad \frac{v_{o2}}{v_{id}} = \frac{1}{2}g_m R_D$$

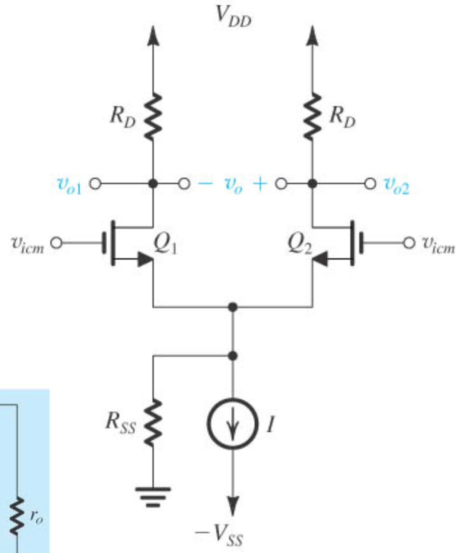
$$A_d \equiv \frac{v_{o2} - v_{o1}}{v_{id}} = g_m R_D$$

6dB

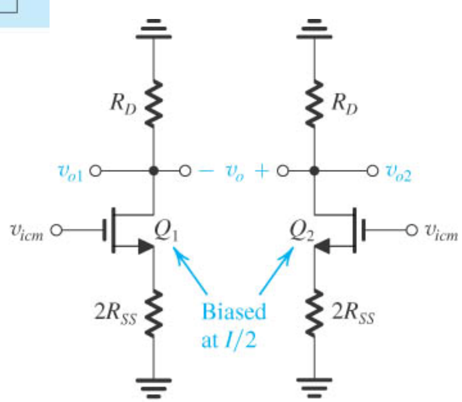
7.2.2 Common-mode gain and common-mode rejection ration



(a)



(a)



(b)

Neglect r_o:

$$i_s = \frac{v_{icm}}{\frac{1}{g_m} + 2R_{ss}}$$

$$v_{o1} = v_{o2} = -i_s R_D = -\frac{v_{icm} R_D}{\frac{1}{g_m} + 2R_{ss}} \cong -\frac{v_{icm} R_D}{2R_{ss}}$$

For single-end output:

$$|A_{cm}| = \frac{v_{o1}}{v_{icm}} = \frac{R_D}{2R_{SS}} \qquad |A_d| = \frac{1}{2} g_m R_D$$

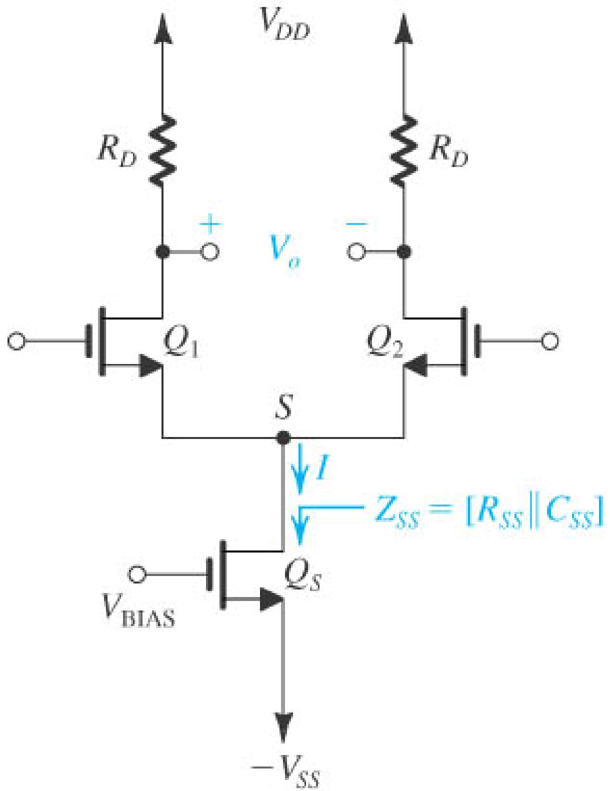
$$\text{CMRR} = \frac{|A_d|}{|A_{cm}|} = g_m R_{SS}$$

For differential output:

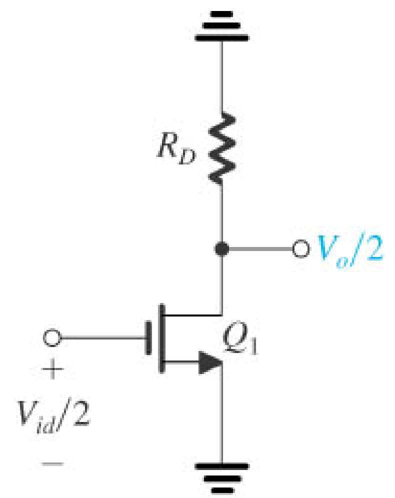
$$|A_{cm}| = \frac{v_{o1} - v_{o2}}{v_{icm}} = 0 \qquad \boxed{\text{CMRR} = \infty}$$

7.6 Frequency Response of the Differential Amplifier

7.6.1 Analysis of the Resistively Loaded MOS Amplifier



(a)



(b)

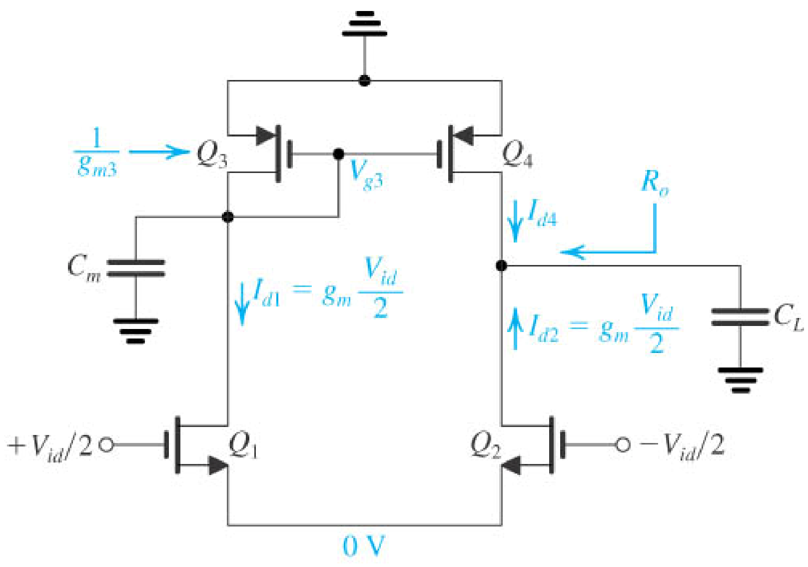
Differential half-circuit:

Common Source Amplifier

R_{SS}*: Output Resistance of *Q_S

***C_{SS}*: C_{dbs}, C_{gds}, C_{sb1}, C_{sb2}**

7.6.2 Analysis of the Active-Loaded MOS Amplifier



(a)

$$C_m = C_{gd1} + C_{db1} + C_{db3} + C_{gs3} + C_{gs4}$$

$$C_L = C_{gd2} + C_{db2} + C_{gd4} + C_{db4} + C_x$$

$$R_O = r_{o2} \,||\, r_{o4}$$

$$g_{m3} = g_{m4}$$

$$V_{g3} = -\frac{g_m V_{id}/2}{g_{m3} + sC_m}$$

$$I_{d4} = -g_{m4} V_{g3} = \frac{g_{m4} g_m V_{id}/2}{g_{m3} + sC_m}$$

$$I_O = I_{d4} + I_{d2}$$

$$= \frac{g_{m4} g_m V_{id}/2}{g_{m3} + sC_m} + g_m (V_{id}/2)$$

$$V_O = I_O \frac{1}{\frac{1}{R_O} + sC_L} = \left(\frac{g_{m4} g_m V_{id}/2}{g_{m3} + sC_m} + g_m (V_{id}/2) \right) \frac{1}{\frac{1}{R_O} + sC_L}$$

$$= g_m R_o \left(\frac{V_{id}}{2} \right) \left(1 + \frac{1}{1 + s\frac{C_m}{g_{m3}}} \right) \frac{1}{1 + sR_o C_L}$$

$$A_d(s) \equiv \frac{V_o}{V_{id}} = g_m R_o \left(\frac{1 + s\frac{C_m}{2g_{m3}}}{1 + s\frac{C_m}{g_{m3}}} \right) \frac{1}{1 + sR_o C_L}$$

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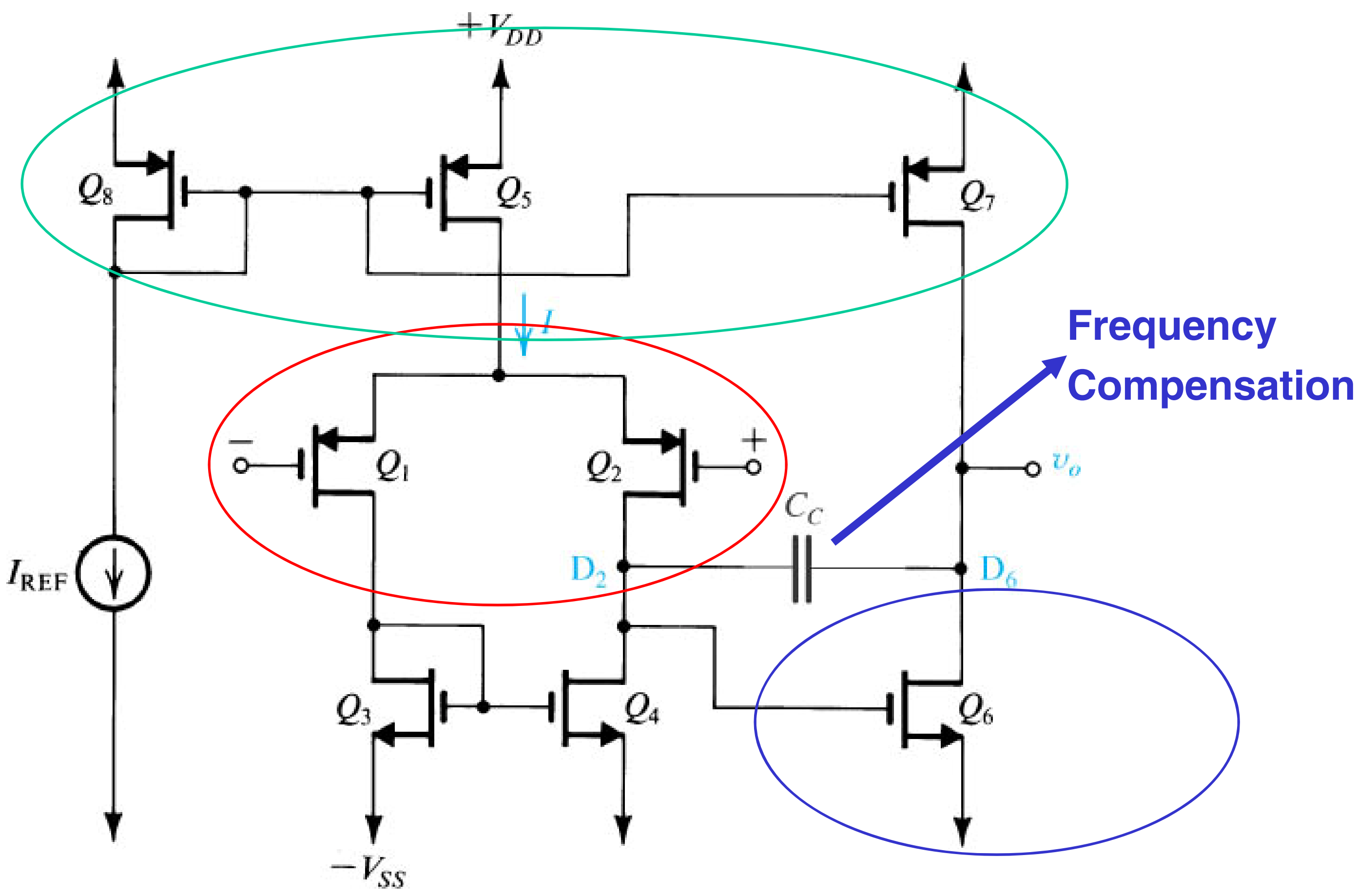
7.7 Multistage Amplifiers

Why Multistage Amplifiers?

- The first stage is usually required to provide a *high input resistance* in order to avoid loss of signal level when the amplifier is fed from a high resistance source
- In a differential amplifier the input stage must also provide *large common-mode rejection*
- The middle stage is to provide the *bulk of the voltage gain*, conversion of the signal from differential mode to single-ended mode, and the shifting of the DC: allow output to swing both positive and negative
- Final stage is to provide a *low output resistance* in order to avoid loss of gain when load resistance is low: source follower / emitter follower

7.7 Multistage Amplifiers

7.7.1 A Two-Stage CMOS Op Amp



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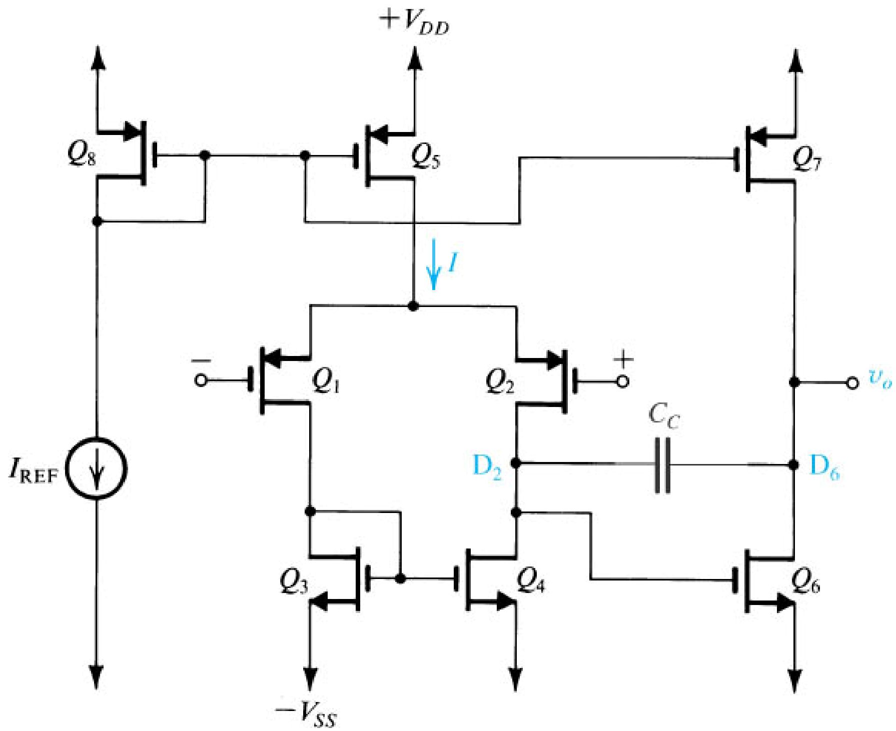
7.7.1 A Two-Stage CMOS Op Amp – Voltage Gain



First Stage:

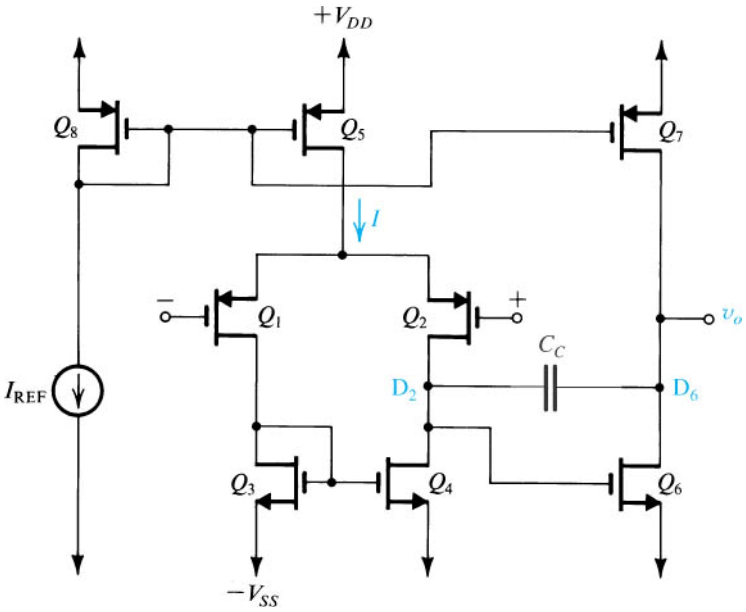
$$A_1 = -g_{m1}(r_{o2} \| r_{o4}) \quad (7.146)$$

Second Stage:

$$A_2 = -g_{m6}(r_{o6} \| r_{o7})$$

Example 7.3

	Q_1	Q_2	Q_3	Q_4	Q_5	Q_6	Q_7	Q_8
W/ L	20/0.8	20/0.8	5/0.8	5/0.8	40/0.8	10/0.8	40/0.8	40/0.8



$$I_{REF} = 90\mu A, V_{tn} = 0.7V, V_{tp} = -0.8V$$

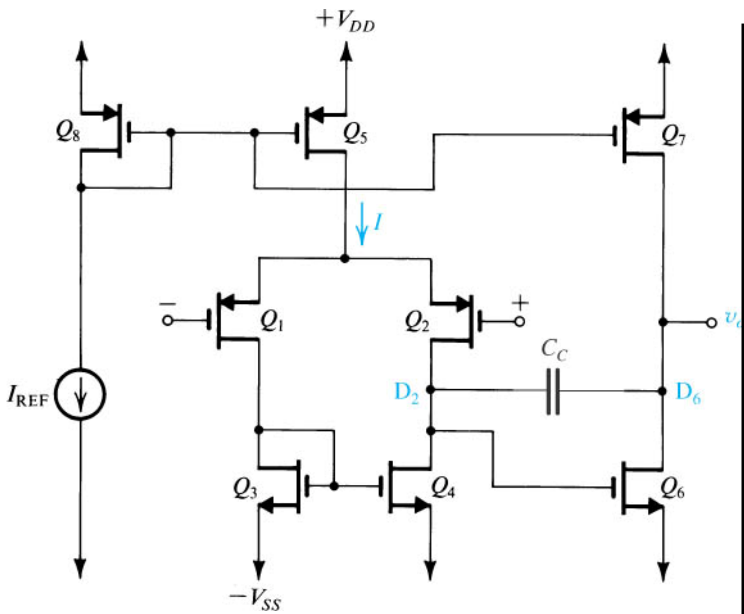
$$\mu_n C_{ox} = 160\mu A/V^2, \mu_p C_{ox} = 40\mu A/V^2$$

$$|V_A| = 10V, V_{DD} = V_{SS} = 2.5V$$

Find I_D, $|V_{OV}|$, $|V_{GS}|$, g_m, r_o, A_1, A_2.

Example 7.3

Find I_D, $|V_{OV}|$, $|V_{GS}|$, g_m, r_o, A_1, A_2.



	Q_1	Q_2	Q_3	Q_4	Q_5	Q_6	Q_7	Q_8
W/ L	20/0.8	20/0.8	5/0.8	5/0.8	40/0.8	10/0.8	40/0.8	40/0.8
I_D(μA)	45	45	45	45	90	90	90	90
$\|V_{ov}\|$(V)	0.3	0.3	0.3	0.3	0.3	0.3	0.3	0.3
$\|V_{GS}\|$(V)	1.1	1.1	1	1	1.1	1	1.1	1.1
g_m (mA/V)	0.3	0.3	0.3	0.3	0.6	0.6	0.6	0.6
r_o (Ω)	222k	222k	222k	222k	111k	111k	111k	111k

$$I_{REF} = 90\mu A, V_{tn} = 0.7V, V_{tp} = -0.8V$$

$$\mu_n C_{ox} = 160\mu A/V^2, \mu_p C_{ox} = 40\mu A/V^2$$

$$|V_A| = 10V, V_{DD} = V_{SS} = 2.5V$$

$$I_D = \frac{1}{2}(\mu_n C_{ox})(W/L)V_{ov}^2 \quad |V_{GS}| = |V_{ov}| + |V_t| \quad g_m = 2I_D/|V_{ov}| \quad r_o = |V_A|/I_D$$

$$A_1 = -g_{m1}(r_{o2} \| r_{o4}) = -33.3V/V$$

$$A_2 = -g_{m6}(r_{o6} \| r_{o7}) = -33.3V/V$$

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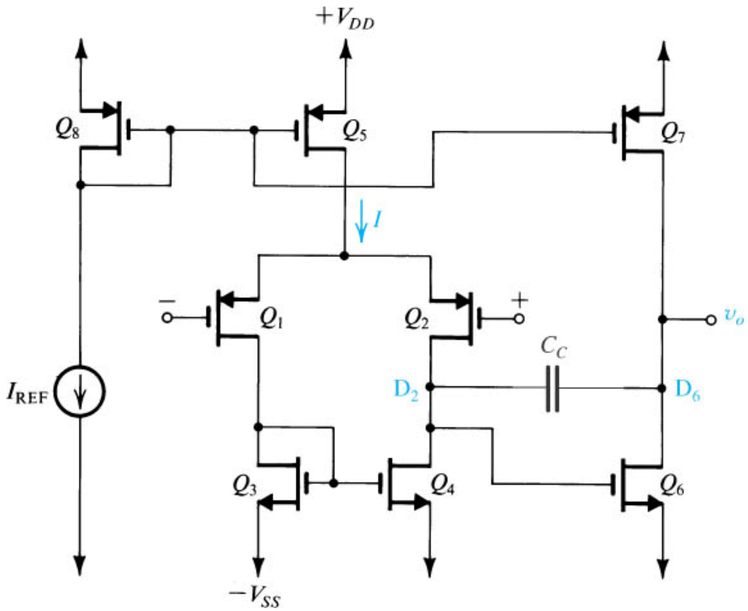
Example 7.3



The lower limit of the input common-mode is the value at which Q_1 and Q_2 leave the saturation region:

$$V_{D1} = -2.5 + 1 = -1.5V$$

$$V_{in\_lower} = -1.5 - 0.8 = -2.3V$$

The upper limit of the input common-mode is the value at which Q_5 leaves the saturation region:

$$V_{SD5} = 0.3V \Rightarrow V_{D5} = 2.5 - 0.3 = 2.2V$$

$$V_{GS1} = -1.1V \Rightarrow V_{G1} = 2.2 - 1.1 = 1.1V$$

$$V_{in\_upper} = 1.1V$$

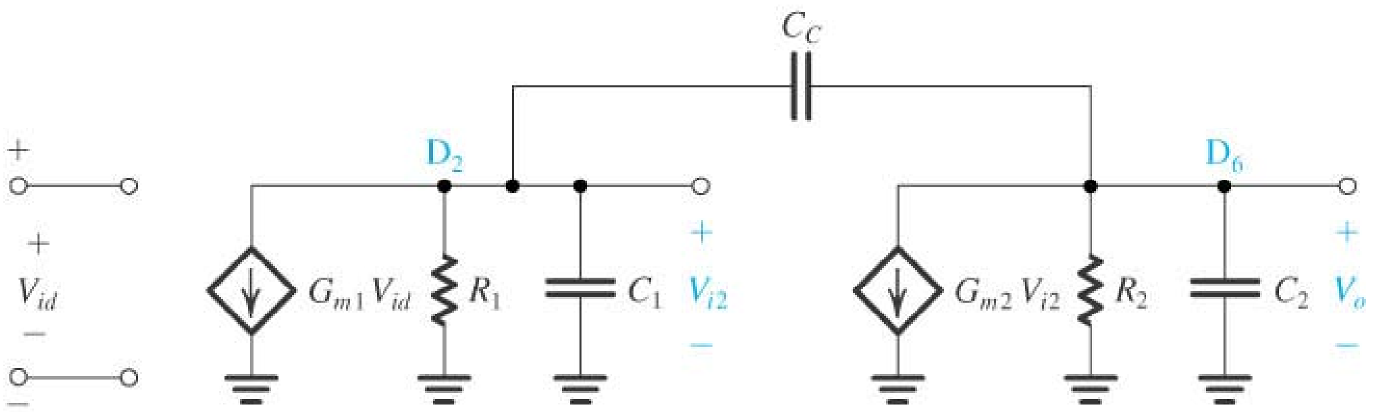
$$v_{GD} \le V_t \Leftrightarrow v_{DS} \ge v_{GS} - V_t \Leftrightarrow v_{DS} \ge V_{OV}$$

$$\text{PMOS}: v_{SD} \ge |V_{OV}|$$

Highest output: $V_{DD} - |V_{OV7}| = 2.5 - 0.3 = 2.2V$

Lowest output: $-V_{SS} + |V_{OV6}| = -2.5 + 0.3 = -2.2V$

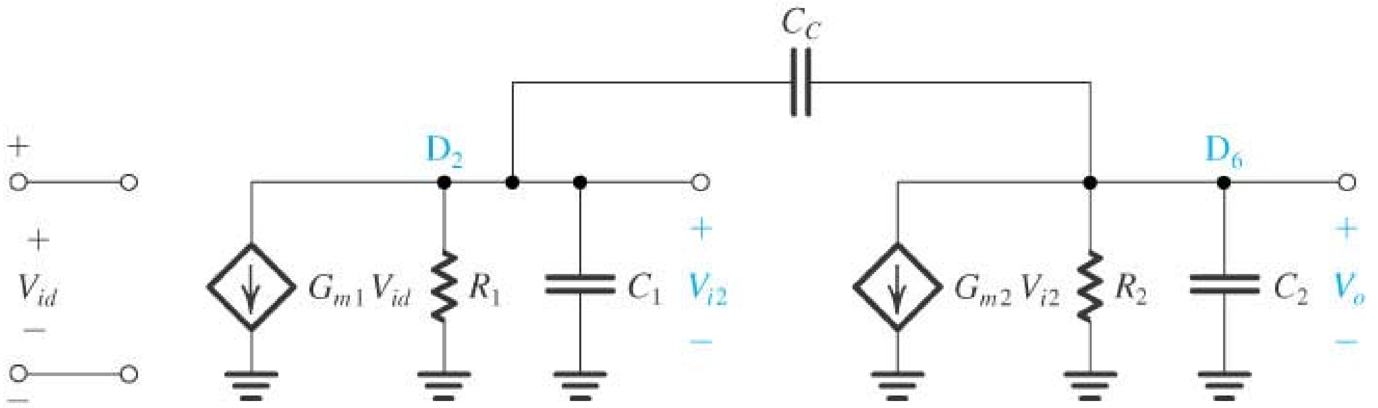
7.7.1 A Two-Stage CMOS Op Amp: Frequency Response



$$C_1 = C_{gd4} + C_{db4} + C_{gd2} + C_{db2} + C_{gs6}$$

$$C_2 = C_{db6} + C_{db7} + C_{gd7} + C_L$$

7.7.1 A Two-Stage CMOS Op Amp: Frequency Response (cont.)



$$G_{m1}V_{id} + \frac{V_{i2}}{R_1} + sC_1V_{i2} + sC_C(V_{i2} - V_o) = 0$$

$$G_{m2}V_{i2} + \frac{V_o}{R_2} + sC_2V_o + sC_C(V_o - V_{i2}) = 0$$

$$\frac{V_o}{V_{id}} = \frac{G_{m1}(G_{m2} - sC_C)R_1R_2}{1 + s[C_1R_1 + C_2R_2 + C_C(G_{m2}R_1R_2 + R_1 + R_2)] + s^2[C_1C_2 + C_C(C_1 + C_2)]R_1R_2}$$

ω_{p1}

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Homework

7.80, 7.85, 7.88, 7.92, 7.93, 7.94, 7.97